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(54) Abstract Title
Integrated circuits provided with self-information

(57) A method of fabricating an integrated circuit includes the steps of fabricating storage means 2 in the integrated circuit, fabricating first connection mean 3-14 which so connects a signal source A, $\overline{A}$ in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and fabricating second connection means 15 connected to the storage means for enabling the reading of the state of the storage means. Pairs of elements 3,4; 7,8 and 11,12 lie in three superposed conductive layers of a semiconductor substrate. A programmable storage means 1B instructs a principal functional part 1 of the integrated circuit to read the contents of the data storage means 2. The data read from the storage means 2 provides information such as a number indicating that the integrated circuit is a revised version or the information may be the fabrication date of the integrated circuit.

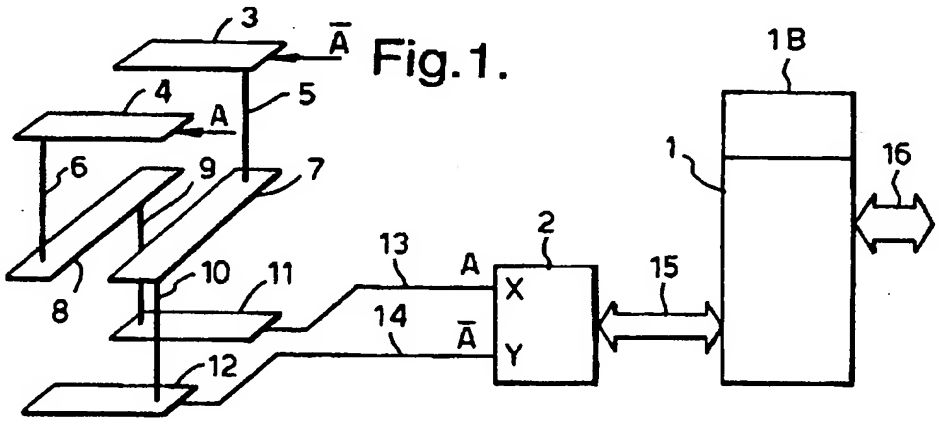

Fig.1.

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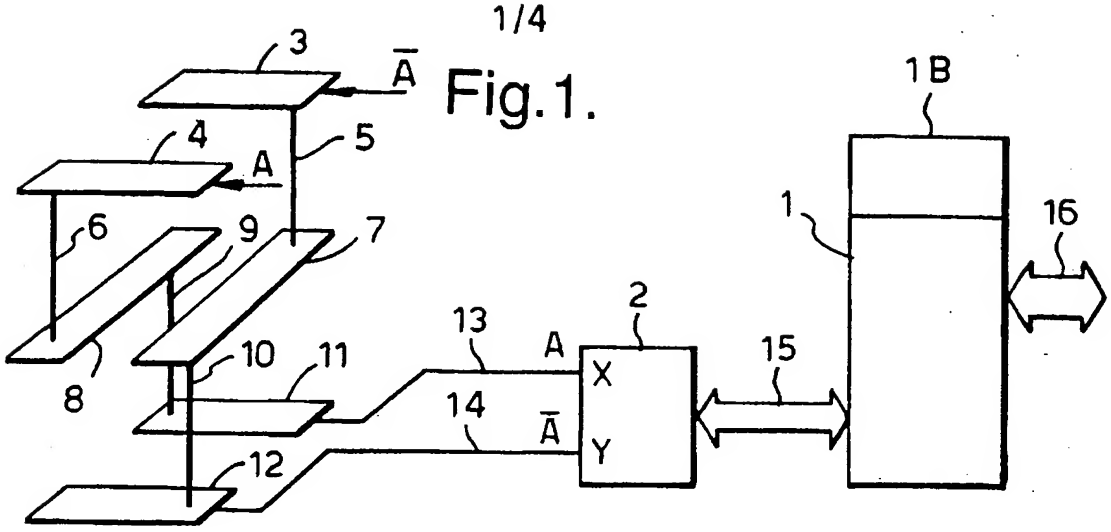


Fig.1.

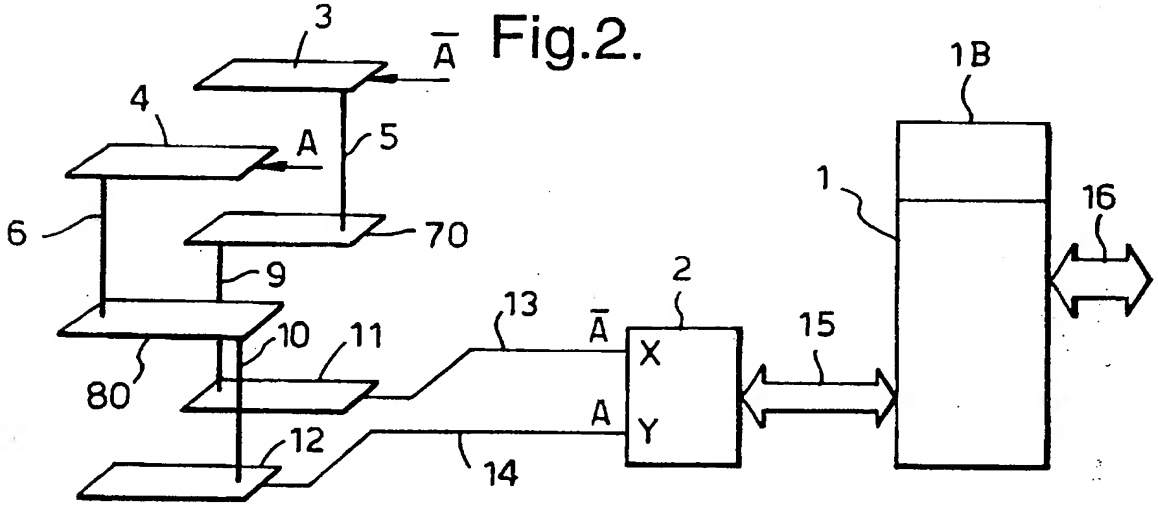


Fig.2.

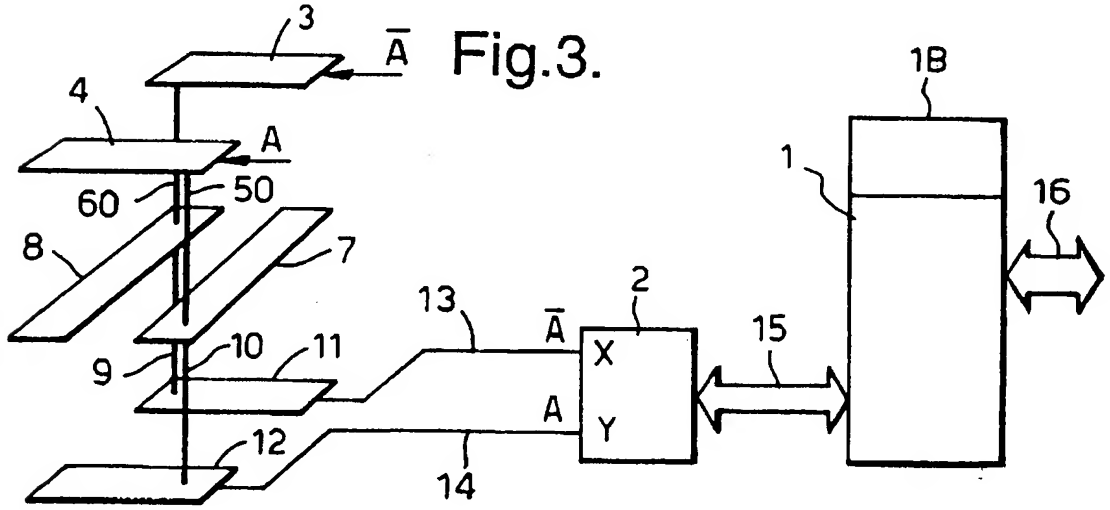
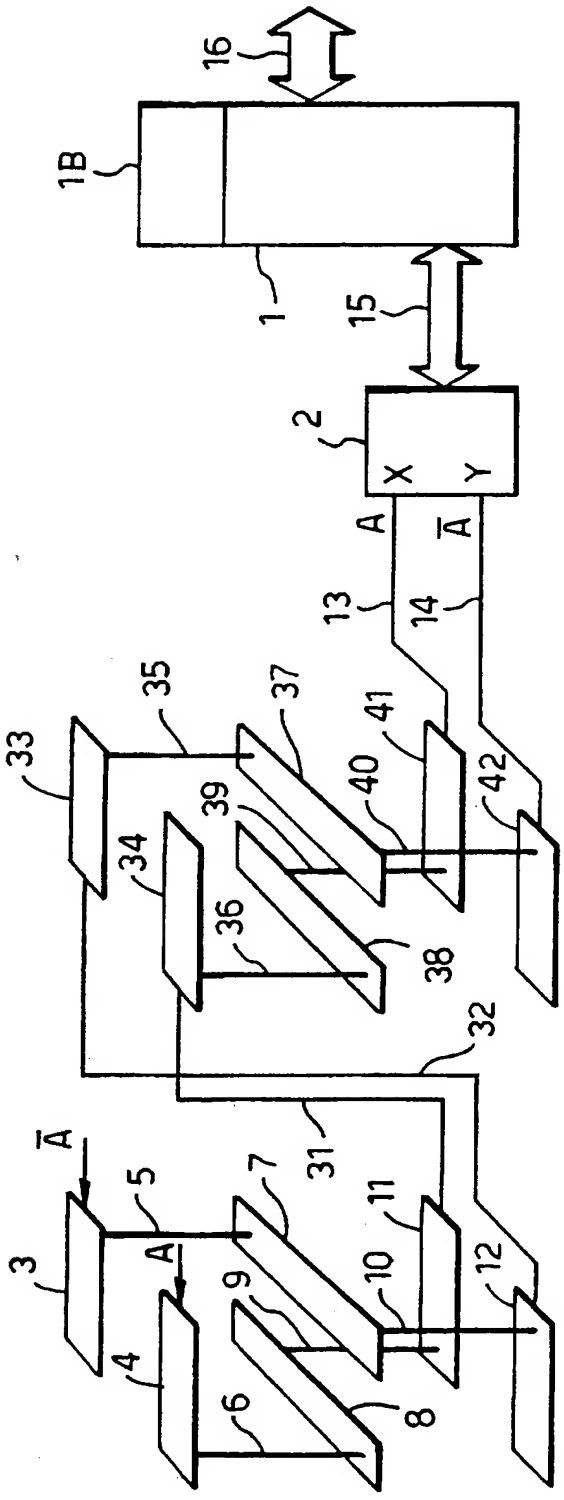


Fig.3.

Fig.4.



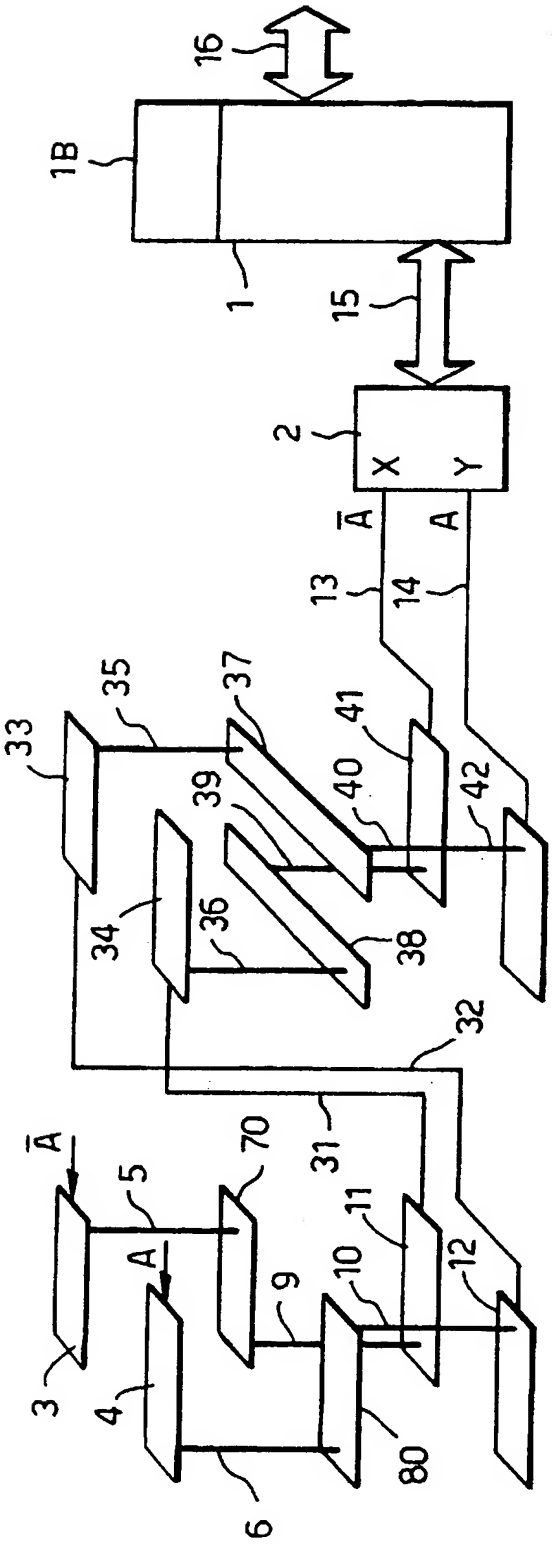
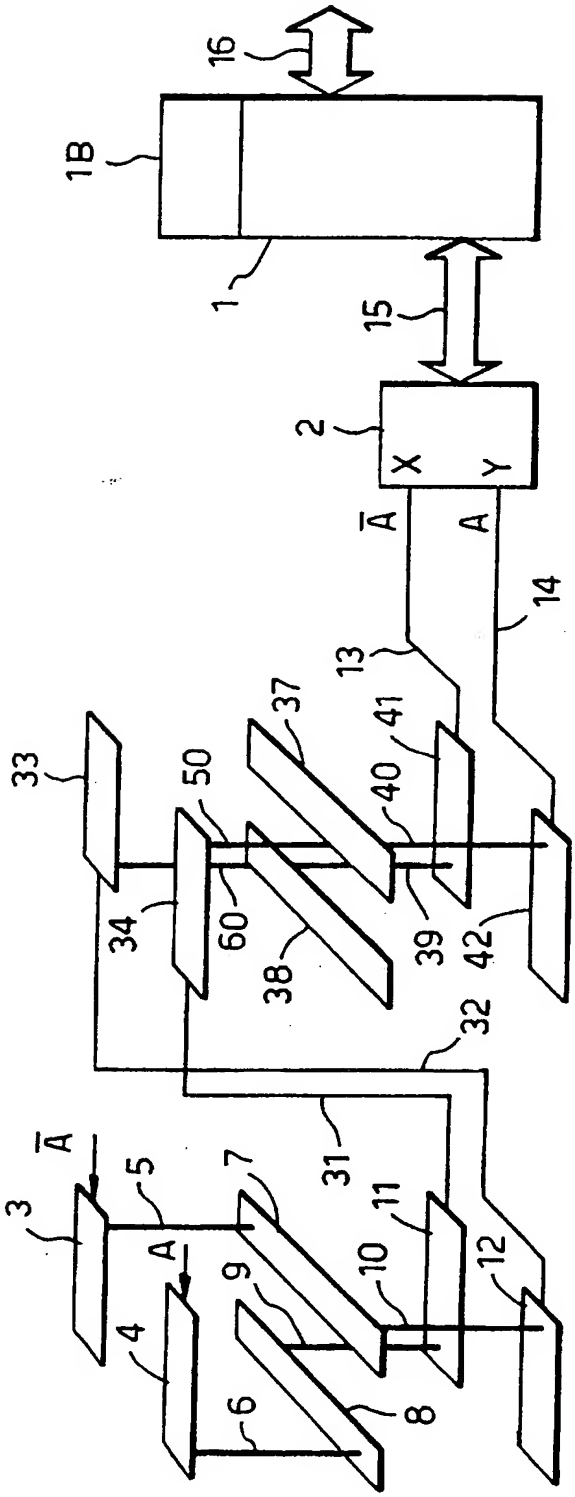


Fig.5.

Fig.6.



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Improvements in or relating to integrated circuits

The invention relates to integrated circuits.

The invention provides a method of fabricating an integrated circuit, including the steps of:

fabricating a storage means in the integrated circuit,

fabricating first connection means which so connects a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

fabricating second connection means connected to the storage means for enabling the reading of the state of the storage means.

Preferably, the second connection means is so fabricated as to enable another component of the integrated circuit to read the state of the storage means.

Alternatively, the second connection means may be so fabricated as to enable another component of the integrated circuit or means external to the integrated circuit to read the state of the storage means.

Preferably, the method of fabricating an integrated circuit includes the steps of:

fabricating a storage means in the integrated circuit,

fabricating programmable storage means in the integrated circuit for storing an operating program for the integrated circuit,

fabricating first connection means which so connects a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

fabricating second connection means so connecting the storage means into the integrated circuit as to permit an operating program stored in the

programmable storage means to enable the reading of the state of the storage means.

Advantageously, in the operation of the integrated circuit under the control of the operating program stored in the programmable storage means, the operating program enables the reading of the state of the storage means in order to determine whether the operating program is being run on the first-produced version of the integrated circuit or a revised version of the integrated circuit and the operating program has the capacity to react to the information obtained from the storage means.

Preferably, the first connection means is fabricated with a first arrangement of its elements in the first-produced version of the integrated circuit and is fabricated with a revised arrangement of its elements in a revised version of the integrated circuit.

Preferably, fabricating the first connection means includes the steps of fabricating a plurality of electrically conductive elements in three layers of the integrated circuit, fabricating electrically conductive interlayer elements connecting the electrically conductive elements in the middle one of the three layers to respective electrically conductive elements in the other layers and fabricating further electrically conductive elements connecting one of the electrically conductive elements in a layer other than the middle layer to an input port of the storage means.

Preferably, fabricating the first connection means includes the steps of fabricating three pairs of electrically conductive elements in three consecutive layers of the integrated circuit, fabricating two pairs of electrically conductive interlayer elements connecting the electrically conductive elements in the middle one of the three layers to respective ones of the electrically conductive elements in the other layers and fabricating a further pair of electrically conductive elements connecting the electrically conductive elements in a layer other than the middle layer to respective input ports of the storage means.

Preferably, the method includes the connection of the signal source to the pair of electrically conductive elements in the layer on one side of the middle layer and the connection of the storage means to the pair of electrically conductive elements in the layer on the other side of the middle layer.

Preferably, in one application of the method, a first arrangement of the elements of the first connection means is changed to a revised arrangement of the elements of the first connection means, for reversing the polarity of the signal source applied to the storage means, by changing the position of the or each electrically conductive element in the middle one of the three layers relative to the other elements of the first connection means.

In an alternative application of the method, the first arrangement of the elements of the first connection means is changed to another revised arrangement of the elements of the first connection means, for reversing the polarity of the signal source applied to the storage means, by changing the position of the or each electrically conductive interlayer element connecting the electrically conductive elements in two adjacent layers relative to the other elements in the first connection means.

When the first connection means includes two pairs of electrically conductive interlayer elements, the first arrangement of the elements of the first connection means may be changed to a revised arrangement of the elements of the first connection means, for reversing the polarity of the signal source applied to the storage means, by changing the position of one pair of electrically conductive interlayer elements relative to the other elements in the first connection means.

Advantageously, the method includes the steps of:

fabricating at least one additional storage means in the integrated circuit,

fabricating an additional first connection means for each additional storage means, the additional first connection means so connecting the signal source to a respective additional storage means that the signal source, when active, sets the state of the respective additional storage means for providing

additional information about the integrated circuit in accordance with the arrangement of elements of the additional first connection means and

fabricating additional second connection means connected to the additional storage means for enabling the reading of the state of the additional storage means.

As before, the additional second connection means may be so fabricated as to enable another component of the integrated circuit or an arrangement external to the integrated circuit or both internal and external arrangements to read the additional storage means.

The inclusion of one additional storage means with its associated first and second connection means in the integrated circuit provides two storage means permitting the indication, for example, of the first-produced, the first revised, the second revised and the third revised versions of the integrated circuit by means of the combined states of the two storage means. Each additional storage means that is included, with its associated first and second connection means, doubles the number of versions, say, of the integrated circuit that may be indicated by means of the combined states of the storage means.

The method may, further, include the steps of fabricating a plurality of first connection means and connecting the plurality of first connection means in a chain between the signal source in the integrated circuit and a storage means.

The method may, further, include the steps of fabricating a plurality of storage means, fabricating a plurality of first connection means for association with each storage means and connecting each plurality of first connection means in a chain between the associated storage means and the signal source in the integrated circuit.

An integrated circuit providing information about itself includes:

a storage means,

first connection means which so connects a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing the information about the

integrated circuit in accordance with the arrangement of the elements of the first connection means and

second connection means connected to the storage means for enabling the reading of the state of the storage means.

Preferably, the second connection means is so fabricated as to enable another component of the integrated circuit to read the state of the storage means.

Alternatively, the second connection means may be so fabricated as to enable an arrangement external to the integrated circuit or both another component of the integrated circuit and an arrangement external to the integrated circuit to read the state of the storage means.

An integrated circuit providing information to itself about itself includes:

a storage means,

programmable storage means for storing an operating program for the integrated circuit,

first connection means so connecting a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing the information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

second connection means so connecting the storage means into the integrated circuit as to permit an operating program in the programmable storage means to enable the reading of the state of the storage means.

Preferably, the arrangement of the elements of the first connection means sets the state of the storage means for providing information as to whether the integrated circuit is a first or a revised version of the integrated circuit and, if a revised version, which version.

Preferably, the first connection means includes a plurality of electrically conductive elements in three layers of the integrated circuit, electrically conductive interlayer elements connecting the electrically conductive elements

in the middle one of the three layers to respective ones of the electrically conductive elements in the other two of the three layers and further electrically conductive elements connecting one of the electrically conductive elements in a layer other than the middle layer to an input port of the storage means.

Preferably, the first connection means includes three pairs of electrically conductive elements in three consecutive layers of the integrated circuit, two pairs of electrically conductive interlayer elements connecting the electrically conductive elements in the middle one of the three layers to respective ones of the other two pairs of electrically conductive elements and a further pair of electrically conductive elements connecting the electrically conductive elements other than the middle pair to respective input ports of the storage means.

Preferably, the pair of electrically conductive elements on one side of the middle pair of electrically conductive elementa is connected to the signal source and the pair of electrically conductive elements on the other side of the middle pair of electrically conductive elements is connected to the storage means.

Advantageously, the integrated circuit includes:

at least one additional storage means,

an additional first connection means for each additional storage means, the additional first connection means so connecting the signal source to the respective additional storage means that the signal source, when active, sets the state of the respective additional storage means for providing additional information about the integrated circuit in accordance with the arrangement of the additional first connection means and

an additional second connection means for each additional storage means, the additional second connection means being so connected to the respective additional storage means as to enable the reading of the state of the additional storage means.

Preferably, the additional second connection means so connect the respective additional storage means into the integrated circuit as to permit another component of the integrated circuit to read the state of the respective additional storage means.

Preferably, programmable storage means is included in the integrated circuit for storing an operating program for the integrated circuit and additional second connection means so connects the additional storage means into the integrated circuit as to enable an operating program in the programmable storage means to enabling the reading of the state of the respective additional storage means.

The integrated circuit may, further, include, a plurality of first connection means connected in a chain between the signal source in the integrated circuit and a storage means.

The integrated circuit may, further, include a plurality of storage means and a plurality of first connection means associated with each storage means, the plurality of first connection means associated with a respective storage means being connected in a chain between the respective storage means and the signal source in the integrated circuit.

The invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 is a diagrammatic representation of a first-produced version of an integrated circuit, including a single first connection means, showing the first connection means in perspective and the remainder of the integrated circuit in the form of a block diagram,

Fig. 2 is a diagrammatic representation of a revised version of the integrated circuit, including a single first connection means, showing a revised arrangement of the first connection means permitting the integrated circuit to identify itself as a revised version,

Fig. 3 is a diagrammatic representation of the revised version of the integrated circuit, including a single first connection means, showing an alternative revised arrangement of the first connection means,

Fig. 4 is a diagrammatic representation of a first-produced version of an integrated circuit including two first connection means,

Fig. 5 is a diagrammatic representation of a revised version of the integrated circuit, including two first connection means, showing a revised arrangement of one of the first connection means permitting the integrated circuit to identify itself as a revised version and

Fig. 6 is a diagrammatic representation of the revised version of the integrated circuit including two first connection means, showing a revised arrangement of the other of the first connection means.

Referring to Fig. 1 of the accompanying drawings, a first-produced version of an integrated circuit includes a principal functional part 1, a programmable storage means 1B belonging to the principal functional part 1, data storage means 2, a plurality of electrically conductive elements 3 to 14 connected together and forming a first connection means of which the elements 13 and 14 are connected to first and second input ports X and Y of the data storage means 2 and second connection means 15 connecting the data storage means 2 to the principal functional part 1 of the integrated circuit which has input-output means 16.

As is known in the semiconductor fabrication art, an integrated circuit includes a plurality of doped regions in specific patterns defining semiconductor devices in a semiconductor block and a plurality of layers which lie on the semiconductor block, the layers including electrically conductive layers which serve principally to interconnect the devices in the semiconductor block. Electrically insulating layers may separate the electrically conductive layers.

The semiconductor block is not shown in Fig. 1 but the elements 3, 4, 7, 8, 11 and 12 lie in three consecutive conductive layers of the semiconductor

block, the elements 7 and 8 lying in the middle one of the three conductive layers, the elements 3 and 4 lying in the layer above the middle conductive layer (as viewed) and the elements 11 and 12 lying in the conductive layer below the middle conductive layer (as viewed), the layers being substantially parallel to one another. The middle-layer elements 7 and 8 are rectangular in shape, of the same dimensions and lie spaced apart with the four longer sides parallel to one other and the shorter sides of each rectangle aligned with the corresponding shorter side of the other rectangle. The elements 3 and 4, too, are rectangular in shape, of the same dimensions and lie spaced apart with the four longer sides parallel to one another and the shorter sides of each rectangle aligned with the corresponding shorter side of the other rectangle. However, the four longer sides of the middle-layer elements 7 and 8 are orthogonal to the four longer sides of the elements 3 and 4. The elements 11 and 12 have the same shape and size as the elements 3 and 4 and, also, occupy the same positions relative to each other as do the elements 3 and 4 relative to each other. The middle-layer elements 7 and 8 fit into a rectangle because of their shape, size and relative positions and, for the same reasons, the elements 3 and 4 fit into a rectangle as do the elements 11 and 12. The elements 3, 4, 7, 8, 11and 12 are so positioned that the rectangles into which they fit are in alignment in the direction orthogonal to the layers. The elements 5, 6, 9 and 10 are interlayer elements. The interlayer element 5 connects the middle-layer element 7 to the element 3 and the interlayer element 10 connects the middle-layer element 7 to the element 12, the interlayer element 6 connects the middle-layer element 8 to the element 4 and the interlayer element 9 connects the middle-layer element 8 to the element 11, the elements 11 and 12 being connected to first and second input ports X and Y of the data storage means 2 by the elements 13 and 14.

In the operation of the first-produced version of the integrated circuit shown in Fig. 1, the element 4 is provided with a digital signal A. As is evident from Fig. 1, the signal A is conducted by the elements 4, 6, 8, 9, 11 and 13 to

the first input port X of the data storage means 2. In a corresponding manner, a digital signal Ã, the complement of A, is supplied to the second input port Y of the data storage means 2 by the elements 3, 5, 7, 10, 12 and 14. The programmable storage means 1B includes a program directing the principal functional part 1 of the integrated circuit to read the contents of the data storage means 2 by way of the second connection means 15 and so find that the signal A is present at the first input port X of the data storage means 2.

The digital signal A and its complement Ã could be provided by a pair of the input supply voltage lines in the integrated circuit.

Referring to Fig. 2 of the accompanying drawings, a revised version of the integrated circuit of Fig. 1 has a first connection means so configured as to supply the signal Ã to the first input port X of the data storage means 2, the signal A being supplied to the second input port Y of the data storage means 2. The change in configuration of the first connection means is achieved by so changing the positions of the middle-layer elements as to reverse the connections between the elements 3 and 4 and the input ports X and Y of the data storage means 2.

Comparing the first connection means of Fig. 2 with the first connection means of Fig. 1, the first connection means of Fig. 2 includes middle-layer elements 70 and 80 in place of the middle-layer elements 7 and 8 of Fig. 1. As shown in Fig. 2, the revised version of the integrated circuit includes the elements 3, 4, 11, 12, 5, 6, 9, 10,13 and 14 which are the same as those elements of Fig. 1 in all respects. The middle-layer element 70 of Fig. 2 is so positioned as to be connected to the element 3 by the interlayer element 5 and to be connected to the element 11 by the interlayer element 9. The middle-layer element 80 of Fig. 2 is so positioned as to be connected to the element 4 by the interlayer element 6 and to be connected to the element 12 by the interlayer element 10. As is shown in Fig. 2, the middle-layer elements 70 and 80 have the same size, shape and relative positions to each other as the elements 3 and 4 and, also, the elements 11 and 12.

In the operation of the revised version of the integrated circuit shown in Fig. 2, a signal Ã is detected at the first input port X of the data storage means 2 when the principal functional part 1 of the integrated circuit is directed to read the contents of the data storage means 2. The program included in the programmable storage 1B means includes information indicating to the integrated circuit that the presence of the Ã signal at the first input port X of the data storage means 2 means that the integrated circuit is a revised version.

It will be understood that the revised configuration of the first connection means in the integrated circuit represented by Fig. 2 compared with the integrated circuit represented by Fig. 1 serves to indicate to the integrated circuit represented by Fig. 2 that it is a revised version, the change in the first connection means not itself being the revision.

Referring to Fig. 3 of the accompanying drawings, an alternative revised configuration of the first connection means in a revised version of the integrated circuit includes interlayer elements 50 and 60 instead of the interlayer elements 5 and 6. The inclusion of the interlayer elements 50 and 60 instead of the interlayer elements 5 and 6 of Fig. 1 has the effect of supplying a signal Ã to the first input port X of the data storage means 2. As shown in Fig. 3, the alternative revised version of the integrated includes the elements 3, 4, 7, 8, 11, 12, 9, 10,13 and 14 which are the same as those elements in Fig. 1 in all respects.

As is shown in Fig. 3, the interlayer element 50 is so positioned as to connect the middle-layer element 7 to the element 4 while the interlayer element 10 connects the middle-layer element 7 to the element 12, the second input port Y of the data storage means 2 being connected to the element 12 by the element 14. The interlayer element 60 is so positioned as to connect the middle-layer element 8 to the element 3 while the interlayer element 9 connects to the middle-layer element 8 to the element 11, the first input port X of the data storage means 2 being connected to the element 11 by the element 13.

In the operation of the revised-version integrated circuit represented by Fig. 3, the signal Ã applied to the element 3 is supplied to the first input port X of the data storage means 2, the signal A applied to the element 4 being supplied to the second input port Y of the data storage means 2.

As is evident from a comparison of Figs. 1 and 3, the change in the configuration of the first connection means is achieved by so changing the positions of the interlayer elements between the middle-layer elements 7 and 8 and the elements 3 and 4 in the layer above the middle layer as to reverse the connections between the elements 3 and 4 and the input ports X and Y of the data storage means 2. As is also evident from Figs, 1 and 3, the reversal in the connection could have been achieved by so changing the positions of the interlayer elements 9 and 10 as to connect the middle-layer element 7 to the element 11 and to connect the middle-layer element 8 to the element 12.

As is shown in Figs. 1, 2 and 3, the different configurations of the first connection means of Figs. 2 and 3 provide the same result and that result differs from the result obtained with the first connection means of Fig. 1, the respective results being detectable by the integrated circuit operating program.

The integrated circuits described with reference to Figs. 1 to 3 are capable of indicating a first-produced version of the integrated circuit by providing a binary signal A at the first input port X of the data storage means 2 and of indicating a revised version of the integrated circuit by providing a binary signal Ã at the first input port X of the data storage means 2. Alternatively, the signal provided at the second input port Y may be used to determine which version of the integrated circuit houses the data storage means 2.

Integrated circuits including two data storage means, two first connection means and two second connection means with one of each of the other components would be capable of indicating a first-produced version of the integrated circuit by providing the binary number AA, say, and indicating revised versions by providing the binary numbers AÃ, ÃA and ÃÃ, from the

first input ports of the two data storage means. Alternatively, the second input ports could be used (providing complementary values to those obtained from the first input ports).

The principles outlined above are applicable to integrated circuits including several data storage elements and first and second connection means, with one of each of the other components, for providing more digits for indicating larger revision numbers.

In each of the arrangements represented by Figs. 1, 2 and 3, satisfactory operation would be obtained by providing signals at the first input port X, alone, of the data storage means 2 by omitting the elements 10, 12 and 14. Also, in the change in the configuration of the first connection means from that shown in Fig. 1 to that shown in Fig. 2, the single middle-layer element 70 could replace the single middle-layer element 8 when only the first input port X of the data storage means 2 is used.

The interlayer elements 5, 6, 9, 10, 50 and 60 included in the integrated circuits represented by Figs. 1 to 3, above, are known in the integrated circuits art as vias.

The rectangle is a convenient shape for the elements 3, 4, 7, 8, 11, 12, 70 and 80 shown in Figs. 1 to 3, above, and so disposing the elements that they fit into rectangles is a convenient arrangement but strict adherence to rectangular forms is not essential in the application of the invention.

Although the elements 3, 4, 7, 8, 11, 12, 70 and 80 could lie in any three consecutive conductive layers of the integrated circuit, the elements are most conveniently located in the three conductive layers closest to the surface of the integrated circuit since, in practice, any revision of the integrated circuit is confined to those layers.

Referring to Fig. 4 of the accompanying drawings, the first-produced version of the integrated circuit including two first connection means includes a first plurality of electrically conductive elements 3 to 12, 31 and 32, a second plurality of electrically conductive elements 33 to 42, 13 and 14, a principal

functional part 1, a programmable storage means 1B belonging to the principal functional part 1, data storage means 2, second connection means 15 and input-output means 16. The principal functional part 1, the programmable storage means 1B, the data storage means 2, the second connection means 15 and the input-output means 16 are the same as those elements in Figs. 1 to 3.

The electrically conductive elements 3 to 12, 31 and 32 serve as one of the first connection means and the electrically conductive elements 33 to 42, 13 and 14 serve as the other of the first connection means. The functions of the electrically conductive elements 3 to 12, 31 and 32 are the same as the functions of the electrically conductive elements 3 to 14, respectively, in Fig. 1. Also, the functions of the electrically conductive elements 33 to 42, 13 and 14 are the same as the functions of the electrically conductive elements 3 to 14, respectively, in Fig. 1. The electrically conductive elements 31 and 32 are connected to the electrically conductive elements 34 and 33, respectively

As is evident from Fig. 4, a signal A applied to the electrically conductive element 4 is conducted by the elements 4, 6, 8, 9, 11, 31, 34, 36, 38, 39, 41 and 13 to the first input port X of the data storage means 2. In a corresponding manner, a signal Ã applied to the electrically conductive element 3 is conducted to the second input port Y of the data storage means 2.

Referring to Fig. 5 of the accompanying drawings, in the revised version of the integrated circuit including two first connection means, in the left-hand first connection means, as viewed, the middle-layer elements 70 and 80 replace the middle-layer elements 7 and 8, respectively, in the left-hand first connection means of Fig. 4, as viewed. The elements in the right-hand first connection means in Fig. 5 remain unchanged in relation to the elements in the right-hand first connection means in Fig. 4, as may be confirmed by comparing the positions and orientations of the elements 33 to 42, 13 and 14 in each figure.

As is evident from Fig. 5, the signal A applied to the electrically conductive element 3 is now conducted to the second input port Y of the data

storage means 2, providing the information that the integrated circuit is a revised version.

In respect of Fig. 5, it is evident that a change made to the right-hand first connection means rather than the left-hand first connection means would have provided the same change to the state of the data storage means 2.

Referring to Fig. 6 of the accompanying drawings, in another revised version of the integrated circuit including two first connection means, in the right-hand first connection means, as viewed, the interlayer elements 50 and 60 replace the interlayer elements 35 and 36, respectively, in the right-hand first connection means of Fig. 4, as viewed. The elements in the left-hand first connection means in Fig. 6 remain unchanged in relation to the elements in the left-hand first connection means in Fig. 4, as may be confirmed by comparing the positions and orientations of the elements 3 to 12, 31 and 32 in each figure.

In respect of Fig. 6, it is evident that a change made to the left-hand first connection means rather than the right-hand first connection means would have provided the same change to the state of the data storage means 2.

In respect of Figs. 4 to 6, the left-hand and right-hand first connection means occupy different positions in the integrated circuit. The ease with which a change could be implemented in one rather than the other of the first connection means would determine whether a left-hand or a right-hand first connection means was changed, taking into account whether it was easier to change the orientations of middle-layer electrically conductive elements or the positions of interlayer electrically conductive elements. There may, of course, be two or more first connection means connected in a chain to each data storage means.

The arrangement represented by Fig. 4 may be modified to include a plurality of data storage means 2 connected to the principal functional part 1 and a left-hand and a right-hand first connection means, in the manner of the Fig. 4 arrangement, connected to each data storage means 2.

Although the information provided by the state of the storage means in the integrated circuits, described above, relates to the revision number of the integrated circuit in which the storage means lies, the information need not relate to the revision number and may, instead, relate to the fabrication date or other information useful to a manufacturer or relevant to the operation of the integrated circuit.

In addition, although the integrated circuits described above provide information for an operating program stored in programmable storage means in the integrated circuit, the second connection means may be such that the information is, alternatively, accessible externally through a boundary scan arrangement, say, or accessible by both a component of the integrated circuit and an external arrangement as included in a boundary scan arrangement, according to the nature of the information.

CLAIMS

1. A method of fabricating an integrated circuit including the steps of:

fabricating a storage means in the integrated circuit,

fabricating first connection means which so connects a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

fabricating second connection means connected to the storage means for enabling the reading of the state of the storage means.

2. A method as claimed in claim 1, including the step of so fabricating the second connection means as to enable another component of the integrated circuit to read the state of the storage means.

3. A method as claimed in claim 1 or claim 2, including the step of so fabricating the second connection means as to enable an arrangement external to the integrated circuit to read the state of the storage means.

4. A method of fabricating an integrated circuit including the steps of:

fabricating a storage means in the integrated circuit,

fabricating programmable storage means in the integrated circuit for storing an operating program for the integrated circuit,

fabricating first connection means which so connects a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

fabricating second connection means so connecting the storage means into the integrated circuit as to permit an operating program in the programmable storage means to enable the reading of the state of the storage means.

5. A method as claimed in any one of claims 1 to 4, including the steps of fabricating the elements of the first connection means with a first arrangement of its elements in a first-produced version of the integrated circuit and fabricating the elements of the first connection means with a revised arrangement of its elements in a revised version of the integrated circuit.

6. A method as claimed in any one of claims 1 to 5, wherein fabricating the first connection means includes the steps of fabricating a plurality of electrically conductive elements in three layers of the integrated circuit, fabricating electrically conductive interlayer elements connecting the electrically conductive elements in the middle one of the three layers to respective electrically conductive elements in the other layers and fabricating further electrically conductive elements connecting one of the electrically conductive elements in a layer other than the middle layer to an input port of the storage means.

7. A method as claimed in any one of claims 1 to 6, wherein fabricating the first connection means includes the steps of fabricating three pairs of electrically conductive elements in three consecutive conductive layers of the integrated circuit, fabricating two pairs of electrically conductive interlayer elements connecting the electrically conductive elements in the middle one of the three conductive layers to respective ones of the electrically conductive elements in the other layers and fabricating a further pair of electrically conductive elements connecting the electrically conductive elements in a layer other than the middle layer to respective input ports of the storage means.

8. A method as claimed in claim 7, including the connection of the signal source to the pair of electrically conductive elements in the layer on one side of the middle layer and the connection of the storage means to the pair of electrically conductive elements in the layer on the other side of the middle layer.

9. A method as claimed in claim 6, wherein a first arrangement of the elements of the first connection means is changed to a revised arrangement of the elements of the first connection means, for reversing the polarity of the signal source applied to the storage means, by changing the position of the or each electrically conductive element in the middle one of the three layers relative to the other elements of the first connection means.

10. A method as claimed in claim 6, wherein a first arrangement of the elements of the first connection means is changed to another revised arrangement of the elements of the first connection means, for reversing the polarity of the signal source applied to the storage means, by changing the position of the or each electrically conductive interlayer element connecting the electrically conductive elements in two adjacent layers in the integrated circuit relative to the other elements in the first connection means.

11. A method as claimed in claim 6 or claim 7, wherein a first arrangement of the elements of the first connection means is changed to a revised arrangement of the elements of the first connection means, for reversing the polarity of the signal source applied to the further storage means, by changing the position of one pair of interlayer elements relative to the other elements of the first connection means.

12. A method as claimed in any one of claims 1 to 11, including the steps of:

fabricating at least one additional storage means in the integrated circuit,

fabricating an additional first connection means for each additional storage means, the additional first connection means so connecting the signal source to the respective additional storage means that the signal source, when active, sets the state of the respective additional storage means for providing additional information about the integrated circuit in accordance with the arrangement of elements of the additional first connection means and

fabricating an additional second connection means for each additional storage means, the additional second connection means being so connected to the respective additional storage means as to enable the reading of the state of the respective additional storage means.

13. A method as claimed in claim 12, including the step of so fabricating the additional second connection means as to enable another component of the integrated circuit to read the state of the additional storage means.

14. A method as claimed in claim 12 or claim 13, including the step of so fabricating the additional second connection means as to enable an arrangement external to the integrated circuit to read the state of the addirional storage means.

15. A method as claimed in any one of claims 1 to 14, including the steps of fabricating a plurality of first connection means and connecting the plurality of first connection means in a chain between the signal source and a storage means.

16. A method as claimed in any one of claims 1 to 14, including the steps of fabricating a plurality of storage means, fabricating a plurality of first

connection means for association with each storage means and connecting each plurality of first connection means in a chain between the associated storage means and the signal source in the integrated circuit.

17. An integrated circuit including:

a storage means,

first connection means so connecting a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

second connection means connected to the storage means for enabling the reading of the state of the storage means.

18. An integrated circuit as claimed in claim 17, including second connection means so connected to the storage means as to enable another component of the integrated circuit to read the state of the storage means.

19. An integrated circuit as claimed in claim 17 or claim 18, including second connection means so connected to the storage means as to enable an arrangement external to the integrated circuit to read the state of the storage means.

20. An integrated circuit including:

a storage means,

programmable storage means for storing an operating program for the integrated circuit,

first connection means so connecting a signal source in the integrated circuit to the storage means that the signal source, when active, sets the state of the storage means for providing information about the integrated circuit in accordance with the arrangement of elements of the first connection means and

second connection means so connecting the storage means into the integrated circuit as to permit an operating program in the programmable storage means to read the state of the storage means.

21. An integrated circuit as claimed in claim 20, wherein the arrangement of the elements of the first connection means sets the state of the storage means for providing information as to which version of the integrated circuit holds the storage means.

22. An integrated circuit as claimed in any one of claims 17 to 21, wherein the first connection means includes a plurality of electrically conductive elements in three layers in the integrated circuit, electrically conductive interlayer elements connecting the elements in the middle one of the three layers to respective elements in the other two of the three layers and further electrically conductive elements connecting one of the electrically conductive elements in one of the three layers other than the middle layer to an input port of the storage means.

23. An integrated circuit as claimed in any one of claims 17 to 22, including three pairs of electrically conductive elements in three consecutive layers in the integrated circuit, two pairs of electrically conductive interlayer elements connecting the middle pair of electrically conductive elements to respective ones of the other two pairs of electrically conductive elements and a further pair of electrically conductive elements connecting a pair of the electrically conductive elements other than the middle pair to respective input ports of the storage means.

24. An integrated circuit as claimed in claim 23, wherein the pair of electrically conductive elements on one side of the middle pair of electrically conductive elements is connected to the signal source and the pair of

electrically conductive elements on the other side of the middle pair of electrically conductive elements is connected to the storage means.

25. An integrated circuit as claimed in any one of claims 17 to 24 including:

at least one additional storage means,

an additional first connection means for each additional storage means, the additional first connection means so connecting the signal source to the respective additional storage means that the signal source, when active, sets the state of the additional storage means for providing additional information about the integrated circuit in accordance with the arrangement of elements of the additional first connection means and

an additional second connection means for each additional storage means, the additional second connection means being so connected to the respective additional storage means as to enable the reading of the state of the respective additional storage means.

26. An integrated circuit as claimed in claim 25, including additional second connection means so connecting the additional storage means into the integrated circuit as to enable another component of the integrated circuit to read the state of the respective additional storage means.

27. An integrated circuit as claimed in claim 25 or claim 26, including programmable storage means for storing an operating program for the integrated circuit and additional second connection means so connecting the additional storage means into the integrated circuit as to enable an operating program in the programmable storage means to enable the reading of the state of the respective additional storage means.

28. An integrated circuit as claimed in claim 17, including a plurality of first connection means connected in a chain between the signal source in the integrated circuit and a data storage means.

29. An integrated circuit as claimed in claim 17, including a plurality of storage means and a plurality of first connection means associated with each of the storage means, the plurality of first connection means associated with a respective storage means being connected in a chain between the respective storage means and the signal source in the integrated circuit.

30. An integrated circuit substantially as herein described with reference to and as shown in Fig. 1 of the accompanying drawings.

31. An integrated circuit substantially as herein described with reference to and as shown in Fig. 2 of the accompanying drawings.

32. An integrated circuit substantially as herein described with reference to and as shown in Fig. 3 of the accompanying drawings.

33. An integrated circuit substantially as herein described with reference to and as shown in Fig. 4 of the accompanying drawings.

34. An integrated circuit substantially as herein described with reference to and as shown in Fig. 5 of the accompanying drawings.

35. An integrated circuit substantially as herein described with reference to and as shown in Fig. 6 of the accompanying drawings.

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Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H1K(KGX)

Int Cl (Ed.6): H01L

Other:

Documents considered to be relevant:

Category	Identity of document and relevant passage	Relevant to claims
A	US 5459355 INTEL	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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